**TITLE: DESIGN OF 16-BIT RISC PROCESSOR**

**ABSTRACT:**

The Reduced Instruction Set Computer or RISC is a microprocessor design principle that favors a smaller and simpler set of instructions that all take same amount of time to execute. RISC architecture is used across a wide range of platforms from cellular phones to super-computers. In this Project the behavioral design and functional characteristics of 16-bit RISC processor is proposed, which utilizes minimum functional units without compromising in performance. The design is based on Harvard architecture having separate data memory and instruction memory. The instruction word length is 24-bit wide. The processor supports 16 instructions with three addressing modes. It has 16 general purpose registers. Each register can store 16-bit data. The processor has 16- bit ALU capable of performing 11 arithmetical and logical operations. The processor also incorporates a flag register which indicates carry, zero and parity status of the result. All the modules in the design are coded in Verilog. The individual modules are designed and tested at each level of implementation and finally integrated in a top level module by appropriate mapping.

**SOFTWARE USED:** Xilinx Vivado

**LANGUAGE USED:** Verilog

**OUTCOMES:**

1. **Design of 16 bit RISC processer by using Verilog language**
2. **Verification of Arthematic and logical and some special operations**
3. **Knowing practically how a processer works**